What is Claimed is:

1. A current signal generating circuit for generating a current source for use by on- or off-chip components, the circuit comprising:

an on-chip output current circuit configured to generate an output current and a reference current based on an input voltage, the output current substantially proportional to the reference current;

an on-chip resistive element coupled to the output current circuit and having a resistance configured to regulate the output current using the reference current, the resistance varying according to a temperature of the resistive element; and

an on-chip temperature compensation circuit coupled to the output current circuit and the resistive element, and configured to compensate for the varying resistance by adjusting the reference current in accordance with the varying resistance of the resistive element.

2. A current signal generating circuit according to Claim 1, wherein the on-chip temperature compensation circuit is configured to compensate for the varying resistance by adjusting the reference current using a current proportional to an absolute temperature of the on-chip resistive element.

3. A current signal generating circuit according to Claim 2, wherein the temperature compensation circuit comprises amplification circuitry configured to generate the current proportional to an absolute temperature of the on-chip resistive element.

4. A current signal generating circuit according to Claim 3, wherein the amplification circuitry comprises first and second transistors coupled to a differential amplifier, the differential amplifier configured to equalize respective current draws of the first and second transistors.

5. A current signal generating circuit according to Claim 4, wherein the first transistor is capable of having eight times less current density as the second transistor.

6. A current signal generating circuit according to Claim 4, wherein an output of the differential amplifier is coupled to the gates of opposing third and fourth transistors, the differential amplifier configured to equalize respective current draws of the first and second transistors using the opposing third and fourth transistors.

7. A current signal generating circuit according to Claim 3, wherein the temperature compensation circuit further comprises current mirror circuitry coupled to the amplification circuitry, and configured to generate a compensation current mirroring

the current proportional to an absolute temperature of the on-chip resistive element to adjust the reference current.

8. A current signal generating circuit according to Claim 1, wherein the temperature compensation circuit is configured to compensate for the varying resistance by bypassing a flow of the reference current through the on-chip resistive element.

9. A current signal generating circuit according to Claim 1, wherein the output current circuit is configured to generate an output current substantially equal to the reference current.

10. A current signal generating circuit according to Claim 1, wherein the on-chip resistive element is an array of on-chip semiconductor resistors.

11. A method of compensating for a current source used by on- or off-chip components, the method comprising:

generating an output current and a reference current based on an input voltage with an on-chip output current circuit, the output current substantially proportional to the reference current;

regulating the output current with the reference current using a resistance of an on-chip resistive element, the resistance varying according to a temperature of the resistive element; and

compensating for the varying resistance with an on-chip temperature compensation circuit coupled to the output current circuit and the on-chip resistive element, and configured to adjust the reference current in accordance with the varying resistance of the resistive element.

12. A method according to Claim 11, wherein compensating further comprises compensating for the varying resistance with an on-chip temperature compensation circuit configured to adjust the reference current according to the temperature of the on-chip resistive element by generating a current proportional to an absolute temperature of the on-chip resistive element.

13. A method according to Claim 12, wherein compensating further comprises compensating for the varying resistance with an on-chip temperature compensation

circuit having amplification circuitry configured to generate the current proportional to the absolute temperature of the on-chip resistive element.

14. A method according to Claim 13, wherein the amplification circuitry comprises first and second transistors coupled to a differential amplifier, the method further comprising equalizing respective current draws of the first and second transistors using the differential amplifier.

15. A method according to Claim 14, wherein the first transistor is capable of having eight times less current density as the second transistor.

16. A method according to Claim 14, wherein an output of the differential amplifier is coupled to the gates of opposing third and fourth transistors, the method further comprising equalizing respective current draws of the first and second transistors using the opposing third and fourth transistors.

17. A method according to Claim 12, wherein compensating further comprises compensating for the varying resistance with an on-chip temperature compensation circuit configured to adjust the reference current according to the temperature of the on-chip resistive element by generating a compensation current mirroring the current proportional to an absolute temperature of the on-chip resistive element.

18. A method according to Claim 11, wherein compensating the regulating of the output current based on a temperature of the on-chip resistive element comprises bypassing a flow of the reference current through the on-chip resistive element.

19. A method according to Claim 11, wherein generating an output current and a reference further comprises generating an output current substantially equal to the reference current.

20. A method according to Claim 11, wherein regulating further comprises regulating the output current with the reference current using a resistance of an on-chip array of semiconductor resistors.